IN THE DRAWINGS:

Please replace the attached Replacement Sheets for their corresponding drawing sheets in the present Application.

REMARKS

Applicant appreciates the time taken by the Examiner to review Applicant's present application. This application has been carefully reviewed in light of the Official Action mailed 10/05/2006. Applicant respectfully requests reconsideration and favorable action in this case.

Drawing Objections

The drawings were objected to as failing to comply with 37 C.F.R. § 1.84. Replacement drawings are concurrently submitted herewith. Applicant respectfully submits that Figures 3, 4 and 6 include the reference signs mentioned in the description. Blocks 11 and 13 in Figure 1 are now labeled. Applicant respectfully submits that the labels in Figures 4 and 6 are now legible. Accordingly, withdrawal of this objection is respectfully requested.

Rejections under 35 U.S.C. § 102

Claims 1-5, 7, 10, 11, 15, 16, 19-21 and 23 stand rejected as anticipated by U.S. Patent No. 4,855,735 ("Webb").

Claim 1

Claim 1 has been amended to incorporate the limitations of Claim 6 which was rejected under 35 U.S.C. §103. Thus, Claim 1 will be addressed under 35 U.S.C. §103, below. As addressed below under 35 U.S.C. §103, Claim 1 is submitted to be novel and nonobvious in light of the cited prior art.

Claims 7 and 23

Claim 7 recites:

> A system comprising:
> a receiver shift register; and
> a feedback circuit coupled to the receiver shift register;
> wherein one or more cells of the receiver shift register are configured to alternatively accept as input either a bit from a preceding cell or a received bit of synchronization data from a transmitter, and
> wherein if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with a corresponding transmitter shift register, wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors such that the integrity of the communications link can be continually monitored.

Claim 7 teaches a receiver shift register configured to accept "synchronization data from a transmitter." Accordingly, the shift register can be loaded with synchronization data from a transmitter and the bit sequence generated by the receiver shift register can be based on the synchronization data from the transmitter. *See* Specification, paragraphs 0008 and 0009. The bit sequence is not fixed but varies depending on the synchronization data sent from the transmitter. *See* Specification, paragraphs 0029 and 0031. This allows for flexibility in the generation of bit sequences. Another benefit of this

invention is that the bit sequence generated by the receiver shift register may be varied over time. *See* Specification, paragraph 0054.

By contrast, Webb teaches "a parallel word of fixed value 10000000 is loaded into the shift register for recirculation." *See* Webb, column 5, lines 10-15. Applicant respectfully submits that this word is "fixed data." *See* Webb, Figure 1 (which equates a word with fixed data: "PARALLEL DATA WORD(FIXED DATA)"). The word does not come from synchronization data from a transmitter and is fixed. Accordingly, Applicant respectfully submits that Claim 7 is novel in light of Webb.

In addition, Webb is drawn to data clock signal recovery whereas the present invention regards identifying "the occurrence of errors in a data transmission from the transmitter." *See* Webb, Abstract. Because the present invention recites identifying the occurrence of errors in a data transmission from a transmitter whereas Webb teaches a method of data clock signal recovery, Applicant respectfully submits that Claim 7 is novel in light of Webb.

For the above reasons, Applicant respectfully submits that Claim 7 and the respective dependant claims are novel in light of Webb and nonobvious in light of the cited prior art.

Claim 23 recites similar claim language: thus for similar reasons, Claim 23 is also submitted to be novel in light of Webb and nonobvious in light of the cited prior art.

Accordingly, withdrawal of this rejection is respectfully requested.

Rejections under 35 U.S.C. § 103

Claims 6, 8, 9, 12-14, 17 and 18 were rejected as obvious over Webb in view of U.S. Patent No. 4,543,657 ("Wilkinson").

In order to establish a prima facie case of obviousness, the Examiner must show: that the prior art references teach or suggest all of the claim limitations; that there is some suggestion or motivation in the references (or within the knowledge of one of ordinary skill in the art) to modify or combine the references; and that there is a reasonable expectation of success. M.P.E.P. 2142, 2143; In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). The Examiner must explain with reasonable specificity at least one rejection – otherwise, the Examiner has failed procedurally to establish a prima facie case of obviousness. M.P.E.P. 2142; Ex parte Blanc, 13 U.S.P.Q.2d 1383 (Bd. Pat Application. & Inter. 1989). When the motivation to combine the teachings of the references is not immediately apparent, it is the duty of the Examiner to explain why the combination of the teachings is proper. Ex Parte Skinner, 2 U.S.P.Q.2d 1788, 1790 (Bd. Pat. App. & Inter. 1986). Applicant respectfully submits Webb and Wilkinson do not teach each of the claim limitations and therefore do not provide sufficient basis for a prima facie case of obviousness.

Claim 1: Claim 1 has been amended to incorporate the limitations of Claim 6 which was rejected under 35 U.S.C. §103. Claim 1 recites:

> A method comprising:
>
> receiving one or more bits of synchronization data from a transmitter in a receiver of a communications link;
>
> loading the one or more bits of synchronization data into a shift register in the receiver, wherein the receiver shift register has a feedback circuit;
>
> if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with a corresponding transmitter shift register, wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors such that the integrity of the communications link can be continually monitored; and
>
> if the receiver shift register is not filled with synchronization data, shifting the loaded synchronization data and loading one or more additional bits of synchronization data into the receiver shift register.

Because Claim 6 was rejected under 35 U.S.C. §103, Applicant respectfully submits that the Examiner has conceded that the limitations of Claim 6 cannot be found in Webb. Furthermore, for reasons set forth in greater detail above, Applicant respectfully submits that Webb does not teach receiving synchronization data from a transmitter or identifying the occurrence of errors in a transmission from the transmitter as recited in Claim 1.

Applicant respectfully submits that the present invention is nonobvious in light of Webb and Wilkinson at least because neither Webb or Wilkinson teach: "wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors such that the integrity of the communications link can be continually monitored."

The present invention teaches monitoring the integrity of a communications link by identifying errors in a transmission from the transmitter. *See* Specification, paragraphs 0004 and 0059. Errors are identified by comparing a plurality of bit sequences received from a transmitter with one or more bit sequences generated by the receiver shift register. *See* Specification, paragraph 0027.

By contrast, Wilkinson teaches using a pseudo-random number generator to produce "a time-spaced sequence of pseudo-random numbers such that each number uniquely represents the time of day." *See* Wilkinson, Abstract. In other words, the pseudo-random number generator of Wilkinson is used to generate a clock. *See* Wilkinson, column 4, lines 15-33. It appears this clock is used to synchronize a "receiver clock modem" with a "transmitter clock modem." *See* Wilkinson, column 5, lines 23-35. The purpose for this synchronization seems to be the improvement of communication systems by ensuring accurate time signal reference. *See* Wilkinson, column 1, lines 25-40 and 49-55. To the extent error checking is done in Wilkinson, it appears that a pseudo-random data sequence generated by receiver shift register 34 is compared to a received input signal to determine if the sequence in the shift register is correct: the comparison of Wilkinson is not done for purposes of analyzing communications link integrity. *See* Wilkinson, column 6, lines 20-40. Thus Wilkinson does not teach identifying "the occurrence of errors such that the integrity of the communications link can be continually monitored."

This fundamental difference between the two systems is borne out by what the identification of errors indicates and the consequent responses of the two different systems. In Wilkinson, if the bit error rate exceeds a threshold, the data in the shift register is deemed to be

corrupt, synchronization is presumed not to have been achieved and a process of re-synchronization occurs. *See* Wilkinson, column 6, lines 30-65. By contrast, in the present invention, identifying the occurrence of errors allows users to continually monitor the integrity of a communications link and repair or replacement of the communication link may occur. *See* Specification, paragraph 0059. Thus, in the present invention, the identification of the occurrence of errors does not result in re-synchronization-as in Wilkinson-but instead may result in the repair/replacement of the communications link itself. Consequently, analyzing communications link integrity as taught by the present invention is very different from the clock scheme of Wilkinson.

Furthermore, the methodology with which the two different systems compare bit sequences is very different. In the present invention, after synchronization of the receiver shift register has been achieved, errors are identified by comparing a plurality of bit sequences received from a transmitter with one or more bit sequences generated by the receiver shift register. *See* Specification, paragraph 0027. The plurality of received bit sequences are interspersed throughout a transmission: thus errors are identified over the course of the transmission. Identifying errors over the course of a transmission allows for the integrity of the communications link to be continually monitored. *See* Specification, paragraph 0059. By contrast, in Wilkinson, comparing a received bit sequence with a bit sequence is part of the process of synchronization and is done to ensure that the correct bits have been loaded into the receiver shift register. *See* Wilkinson, column 6, lines 53-68. After synchronization has been achieved, there is no further need to compare bit sequences and the receiver pseudo-random number generator is thereafter used to generate a clock. *See* Wilkinson, column 7, lines 35-50. Thus, Applicant respectfully submits that Wilkinson does not teach "during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission."

As a corollary to the above, interspersing bit sequences in a transmission allows the integrity of a communications link to be "continually monitored." Applicant respectfully submits that Wilkinson does not teach continually monitoring the integrity of a communications link.

An additional point of differentiation between the present invention and Wilkinson is that it appears that because the shift register of Wilkinson is used as a clock, the shift register length is determined by the amount of time that must be clocked, i.e. in Wilkinson a 25-stage shift register is used to increment a 24 hour period. *See* Wilkinson, column 4, lines 25-50. Because the shift register of the present invention is used for a fundamentally different purpose,

namely, generating a bit sequence for comparison with a received bit sequence, the length of the shift register is not so constrained.

For similar reasons, Claims 7 and 23 are also submitted to be nonobvious in light of Webb and Wilkinson.

For the above reasons, Applicant respectfully submits that Claim 1 and the respective dependant claims are nonobvious in light of Webb and Wilkinson. Accordingly, withdrawal of this rejection is respectfully requested.

CONCLUSION

Applicant respectfully requests that the Examiner withdraw his rejections of Claims 1, 7 and 23 and the respective dependant claims. Applicant has now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims 1-5, 7-17 and 19-23. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

An extension of one (1) month is requested and a Notification of Extension of Time Under 37 C.F.R. § 1.136 with the appropriate fee is enclosed herewith.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-3183 of Sprinkle IP Law Group.

Respectfully submitted,

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